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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,968	09/24/2003	Shuuichi Ueno	243074US2DIV	1474

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EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 10/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,968	UENO ET AL.	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/24/03 and 11/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 are cancelled in the amendment dated 24 Sep 2003.

Drawings

2. Figure 36 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 9-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6211045 to Liang in view of US 6498374 to Ohuchi

Regarding claim 8, Liang discloses a method of manufacturing a semiconductor device comprising the steps of:

(a) successively depositing an oxide film 21, column 3 line 1, fig. 1 step 12, and a conductive layer 31, column 3 line 16, on a semiconductor substrate 20, fig. 3,

(b) patteming said conductive layer 31 to form a gate electrode, fig. 4, by performing the step (b), said oxide film 21 being made thinner in thickness in an out-of-gate electrode region where said gate electrode is not formed, fig. 4,;

(c) forming an oxidation inhibiting layer 21 composed of an antioxidant (nitridized layer 21), column 3 lines 5-6, fig. 1 step 13, between said oxide film 21 said semiconductor substrate 20 in said out-of-gate-electrode region.

(d) perfonning an oxidation processing, fig. 1 step 16, column 3 line 31-40, over the entire surface of semiconductor substrate after the step (c) ; and

(e) introducing impurity of a predetermined conductivity by using said gate electrode as a mask, to form a source/drain region in the surface of said semiconductor substrate, wherein a MOS transistor is made up of said gate electrode 42, oxide film 41 underlying gate electrode 42 and source/drain region, by performing the step (d), said oxide 41 underlying gate electrode 42 is formed on the side surface of said gate electrode 42 and is

made thicker in thickness under the edge (region 51 and 52), fig. 5, proximity than the under the central portion of said gate electrode 42, and oxide film 41 in said out-of-gate-electrode region is made thinner in thickness than oxide film 41 to be formed on the side surface (region 51 and 52) of said gate electrode 42.

With respect to anti oxidation layer, Liang discloses identical or substantially identical processes produce the MOS, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977). In addition, such anti oxidation layer can be seen in fig. 17-18 of US 6498374 to Ohuchi.

With respect to 'introducing impurity of a predetermined conductivity by using gate electrode as a mask, to form a source/drain (S/D) region in the surface of semiconductor substrate', Liang obviously discloses such S/D regions in the MOS transistor, because such S/D formation process is typical in the art, see Ohuchi's reference fig. 2-A.

Regarding claim 9, Liang does not discloses the method wherein by performing the step (d), oxide film 21 in said out-of-gate-electrode region is made thinner in thickness than oxide film 41 underlying the central portion of said gate electrode 42.

But, Liang discloses the oxide film 21 in said out-of-gate-electrode region has general thickness. In addition, Ohuchi reference discloses the oxide film 28a in said out-of-gate-electrode region 27 is made thinner in thickness than oxide film 25 underlying the central portion of said gate electrode 27, fig. 18. Accordingly, it would have been obvious to one of ordinary skill in art to use the thickness teaching of Ohuchi with Liang's thickness in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the

optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 10, Liang does not discloses the method wherein the step (c) includes the step of implanting atom above gas having an oxidation inhibiting function and having higher reactivity with said semiconductor substrate than said oxide film by using said gate electrode as a mask, to form said oxidation inhibiting layer.

However, Ohuchi reference discloses the includes the step of implanting atom above gas having an oxidation inhibiting function and having higher reactivity with said semiconductor substrate than said oxide film by using said gate electrode as a mask, to form said oxidation inhibiting layer, fig. 2-B and fig 16-18. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the oxidation teaching of Ohuchi with Liang's process, because it would have suppressed the increase in a thickness of the gate insulating film toward the semiconductor substrate, and hence lowering of a gate voltage can be prevented as taught by Ohuchi, see abstract.

Regarding claim 11, Liang discloses a method of manufacturing a semiconductor device comprising the steps of:

(a) successively depositing an oxide film 21 and a conductive layer 31 on a semiconductor substrate 20, fig. 1 and 3;

(b) patterning said conductive layer to form a gate electrode 42, fig. 4;

(c) forming a first oxidation inhibiting layer composed of an antioxidant on the side surface of said gate electrode (layer 41 and 21 comprises nitride and oxide), fig. 1 step 13;

(d) performing an oxidation processing over the entire surface of said semiconductor substrate after step (c); and (e) introducing impurity of a predetermined conductivity by using said gate electrode as a mask, to form a source/drain region in the surface of said semiconductor substrate, wherein a MOS transistor is made up of gate electrode 43, oxide film 41underlying gate electrode 42 and source/drain region, by performing the step (d), said film 41 underlying said gate electrode 42 is formed on the side surface of gate electrode (region 51 and 52) and is made thicker in thickness under the edge proximity than under the central portion of said gate electrode, fig. 5, and oxide film 53 to be formed on the side surface of said gate electrode 42 is made thinner in thickness than oxide film 41 underlying the central portion of said gate electrode 42.

With respect to 'introducing impurity of a predetermined conductivity by using gate electrode as a mask, to form a source/drain (S/D) region in the surface of semiconductor substrate', Liang obviously discloses such S/D regions in the MOS transistor, because such S/D formation process is typical in the art, see Ohuchi's reference fig. 2-A.

Regarding claim 12, Liang discloses the method wherein the step (b) includes the step of allowing part of conductive layer to remain in an out-of-gate-electrode region corresponding to the area except for the region for forming gate electrode, fig. 4, and the step (c) further includes the step of removing conductive layer 31 and first oxidation inhibiting layer in said out-of-gate-electrode region after forming first oxidation inhibiting layer, fig. 3.

Regarding claims 13-14, Liang discloses the method wherein the step (c) includes a thermal treatment, column 3 lines 2-8.

With respect to step (e) includes the steps of: (e-1) introducing impurity of said predetermined conductivity at a first impurity concentration; and (e-2) introducing impurity of said predetermined conductivity at a second impurity concentration higher than said first impurity concentration, and the step (e-1) is performed before the step (c), wherein the step (e) includes the steps of: (e-1) introducing impurity of said predetermined conductivity at a first impurity concentration; and (e-2) introducing impurity of said predetermined conductivity at a second impurity concentration higher than said first impurity concentration, and the step (e-1) is performed after the step (d). Such LLD S/D formation is typical in the art as it being disclosed by Ohuchi, in fig. 2-A.

Regarding claim 15, Liang discloses the method wherein the step includes the step of supplying gas having an oxidation inhibiting function and reacting with said conductive layer including said gate electrode, fig. 1 step 17 and fig. 5.

Regarding claims 16-17, the method wherein by performing the step where oxide film 11 is made thinner in thickness in an out-of-gate- electrode region, fig. 4, where gate electrode 42 is not formed, the step (c) includes the step of forming a second oxidation inhibiting layer, step 17 in fig. 1, composed of an antioxidant between said oxide and said semiconductor substrate film in said out-of-gate- electrode region, and by performing the step (d), said oxide film in said out-of-gate-electrode region is made thinner in thickness than oxide film to be formed under the central portion of said gate electrode, wherein the step includes the step of supplying gas, column 3 line 35 and 45, having an oxidation inhibiting function, fig. 1 step 17, reacting with said gate electrode and having higher reactivity with semiconductor substrate than oxide 21.

Liang discloses product that is identical or substantially identical in structure or composition, or are produced by identical or substantially identical processes, a *prima facie* case of either anticipation or obviousness has been established. *In re Best*, 195 USPQ 430, 433 (CCPA 1977).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
07 Oct. 2004

LONG PHAM
PRIMARY EXAMINER